Re-configurable Electronics Behavior Under Extreme Thermal Environment

Adrian Stoica, Veronica Lacayo, Ramesham Rajeshuni,
Didier Keymeulen, Ricardo Zebulum, Joe Neff*, Gary Burke, and Taher Daud

Jet Propulsion Laboratory-NASA, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109, USA
*SPAWAR Systems Center, San Diego, CA
e-mail: *Rajeshuni.Ramesham@jpl.nasa.gov*; ***Tel***: 818 354 7190

Abstract

Future NASA missions for Moon and Mars will require fault tolerant electronics to work under extreme temperature environment. We present experimental results with both re-configurable analog and re-configurable digital devices operating between -196°C and +120°C. The re-configurable analog devices tested were the JPL-developed Field Programmable Transistor Arrays (FPTA), and the reconfigurable digital device tested was Virtex II Pro - a Xilinx Field Programmable Gate Array (FPGA). The devices operated successfully within this elongated temperature range. While previous evolvable hardware experiments under extreme temperature environment involved reconfiguration-based recovery of analog FPTA, the interfacing digital electronics that had the reconfiguration algorithms running on them were kept at room temperature. The results point us to combine the analog and digital hardware for operation under an elongated temperature range.

Introduction

Future NASA missions to Moon, Mars and Beyond will face Extreme Environments (EE), including environments with large temperature swings, such as between -180°C and 120°C at the initial landing sites on the Moon, low temperatures of -220 °C to -230°C during the polar/crater Moon missions, and -180°C for Titan in-situ mission. High temperatures of 460 °C will be encountered for Venus Surface Exploration and Sample Return mission. High radiation levels will be faced for Jupiter's Moons missions: 5MRad Total Ionizing Dose (TID) for Europa Surface and Subsurface mission. These extreme environments induce drifts, degradation, or damage into electronic devices.

The current approach for space electronics designs is to use commercial/military range electronics protected through passive (insulation) or active thermal control, and high weight shielding for radiation reduction. This adds to sizable weight and volume, compounded by power loss, and additional cost for the mission. More importantly, as missions will target operations with smaller instruments/rovers and operations in areas without solar exposure, these approaches become infeasible. In many cases the electronics must be collocated with the sensor or actuator in the extreme environment, without the option of being insulated or shielded properly. Therefore, developing EE-electronics would have several advantages including lower costs, less power, and offering in some cases, the only reasonable solution.

Conventional approaches to Extreme Environment Electronics include *hardening-by-process* (HBP), i.e. fabricating devices using materials and device designs with higher tolerance to EE, (e.g using special materials like Silicon Carbide for high temperatures, or Silicon-on Insulator for radiation). Another promising approach is *hardening-by-design* (HBD), i.e. use of special design/compensation schemes. For example, circuit techniques, such as auto-zero correction, are used to alleviate the problem of the (temperature dependent) offset voltages in Operational Transconductance Amplifiers (OTA) operated at low temperatures [1]. Both these hardening approaches are limited, in particular for analog electronics, by the fact that current designs are fixed and, as components are affected by EE, these drifts alter functionality.

A recent approach pioneered by JPL is to mitigate drifts, degradation, or damage on electronic devices in EE by using re-configurable devices and an adaptive self-reconfiguration of circuit topology. This new approach, referred here as hardening-by-reconfiguration (HBR) mitigates drifts, degradation, or damage on electronic devices in EE by using reconfigurable devices and an adaptive self-reconfiguration of circuit topology. In HBR, although device parameters change in EE, while devices still operate (albeit on a different point of their characteristic) a new circuit design, suitable for new parameter values, is mapped into the reconfigurable system to recover the initial circuit functionality. Partly degraded resources are still used, while completely damaged resources are bypassed. The new designs, suitable for various environmental conditions, can be determined prior to operation or determined in-situ by reconfiguration algorithms running on a built-in digital controller.

The scope of this paper is on HBR for low-temperatures, since other studies have been performed for high temperatures and radiation environments [2]. The application here described encompasses the separate testing of the whole Evolvable Hardware system (Evolutionary Processor + Re-configurable chip) at low temperatures, following the assumption that the entire system will be exposed to the space EE. In the experiments, we demonstrate the evolution and recovery of circuits at liquid nitrogen temperatures (-196.6°C) and verify the operational limitation of the evolutionary processor at low temperatures. This adds to our previous experiments where only the re-configurable chip was exposed to EE [2].

The Stand-Alone Board Level Evolvable (SABLE) system [3] designed by JPL is used in the experiments described in this paper. This system is constituted by a DSP working as an evolutionary processor and a reconfigurable mixed signal chip, the FPTA. Section 2 of this paper overviews the SABLE system. Section 3 describes the experiments and section 4 concludes the work.

Overview of SABLES

SABLES integrates an FPTA and a DSP implementing the Evolutionary Platform (EP) as shown in Figure 1. The system is stand-alone and is connected to the PC only for the

purpose of receiving specifications and communicating back the results of evolution for analysis [3].

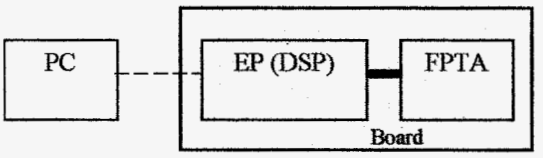


Fig. 1. Block diagram of a simple stand-alone evolvable system.

The FPTA has transistor level reconfigurability, consisting of an 8x8 array of reconfigurable cells. Each cell has a transistor array as well as a set of other programmable resources, including programmable resistors and static capacitors. Figure 2 provides a detailed view of the reconfigurable transistor array cell. The reconfigurable circuitry consists of 14 transistors connected through 44 switches and is able to implement different building blocks for analog processing, such as two- and three-stage OpAmps and Gaussian computational circuits. Details of the FPTA-2 can be found elsewhere [2,3].

The evolutionary algorithm is implemented in a DSP that directly controls the FPTA-2, together forming a board-level evolvable system with fast internal communication ensured by a 32-bit bus operating at 7.5MHz. Details of the EP were presented in [4]. Over four orders of magnitude speed-up of evolution was obtained on the FPTA-2 chip compared to SPICE simulations on a Pentium processor (this performance figure was obtained for a circuit with approximately 100 transistors; the speed-up advantage increases with the size of the circuit).

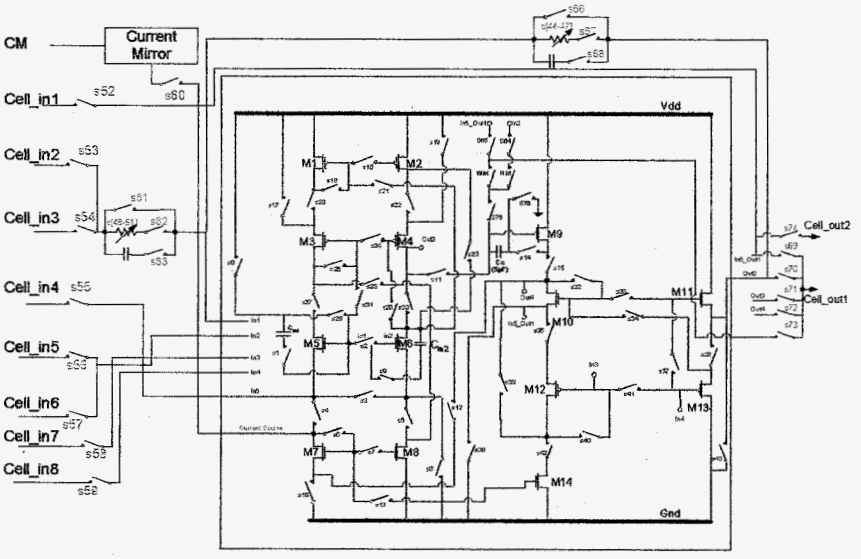


Figure 2: Schematic of the FPTA-2 Cell.

Low Temperature Experiments

This paper focuses on analog/digital electronics at low-temperatures [5]. The experiments cover separate tests of the whole Evolvable Hardware system: the Evolutionary Processor (the DSP in the SABLE system), Xilinx Virtex II Pro FPGA evaluation board, and the Reconfigurable analog array components tested at low and high temperatures.

DSP Tests at low-temperatures

Previous experiments focused exclusively on the tests of the FPTA chips at extreme environments. However, no tests have been reported so far on the behavior of the Evolutionary Processors (EP) at extreme environments. This particular experiment focuses on low-temperature characterization of the DSP working as the EP.

A 320C6701 DSP was tested in a board fabricated by Innovative Integration (SBC62). The board communicates with a PC through a JTAG connection. During the test only the DSP board was placed on the low-temperature chamber: the PC and the JTAG were outside. The FPTA chip was not used in this arrangement.

The DSP was tested by running a simple GA whose target was a simple optimization problem (the maximization of the number of '1's in the chromosomes). This problem is solved in less than 1 minute, after 464 generations. The GA results are deterministic, i.e., the same for each run.

The temperature of the chamber/test article has been driven to 0°C with a scan rate of 5°C/min from room temperature. The dwell time at 0°C temperature was for 8 minutes and electrical measurements were made during this time. Later, the temperature of the chamber has been driven to –30°C, –60°C, –90°C, –120°C at a scan rate of 5°C/min and electrical measurements were made respectively during the dwell (Figure 3).

A Failure was observed during the testing at –120°C step. Electrical measurements were made at –90°C again and the DSP regained its characteristics. This procedure was repeated again: the temperature was driven to –90°C, –100°C, –110°C and –120°C to narrow/identify the temperature range where it failed. The dwell time at each temperature was for 5 minutes and electrical measurements were made during this time. The DSP was functioning at –90°C, –100°C, and –110°C. The failure was again observed during the testing in a temperature range of –110°C to –120°C. During the failure the DSP did not communicate with the PC. The PC-DSP communication link was the only means to read out the DSP outputs in this experiment.

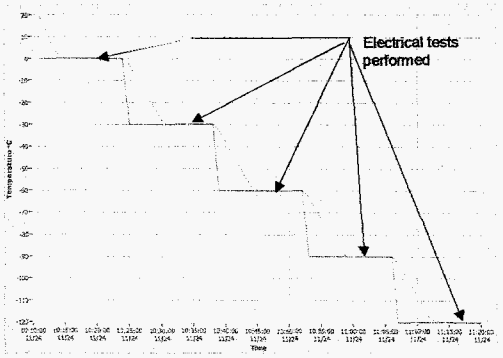


Figure 3: Temperature Profile in the DSP Test.

Other Evolutionary Processors implementations, including FPGAs and other DSP models, will be tested. The final goal of the experiments is to have an implementation operational at -180°C or below.

Half-Wave Rectifier

The low temperature testbed for these experiments used liquid nitrogen, establishing a temperature of -196.6°C. In order to study the effect of low temperatures on the FPTA device only (the DSP was at room temperature), the chip was placed on a separate board that was immersed into liquid nitrogen. This setup did not allow a control for intermediate temperatures between room ambient and liquid nitrogen as described in the previous experiment. A standard ceramic package was used for the chip. A half-wave rectifier was then evolved at -196.6°C with the following setup.

The fitness function given below does a simple sum of errors between the target function and the output from the FPTA. The input was a 2 kHz excitation sine wave of 2V amplitude, while the target waveform was the rectified sine wave. The fitness function rewarded those individuals exhibiting behavior closer to target (by using a sum of differences between the response of a circuit and the target) and penalized those farther from it. The fitness function was:

$$F = \sum_{t_s=0}^{n-1} \begin{cases} R(t_s) - S(t_s) & \text{for } (t_s < n/2) \\ R(t_s) - V_{\max}/2 & \text{otherwise} \end{cases}$$

where $R(t_s)$ is the circuit output, $S(t_s)$ is the circuit stimulus, n is the number of sampled outputs, and V_{max} is 2V (the supply voltage). The output must follow the input during half-cycle, staying constant at a level of half way between the rails (1V) in the other half. After the evaluation of 100 individuals, these were sorted according to fitness and a 9% (elite percentage) portion was set aside, while the remaining individuals underwent crossover (70% rate), either among themselves or with an individual from the elite, and

then mutation (4% rate). The entire population was then reevaluated. The experiment used 2 cells and was run for 300 generations.

The oscilloscope caption is shown in Figure 4a. This was not a robust solution (and it was not even expected to be, since evolutionary algorithm was not asked, through the fitness function, to respond to an entire temperature range) and when taken out to room temperature the response deteriorated as shown in Figure 4b.

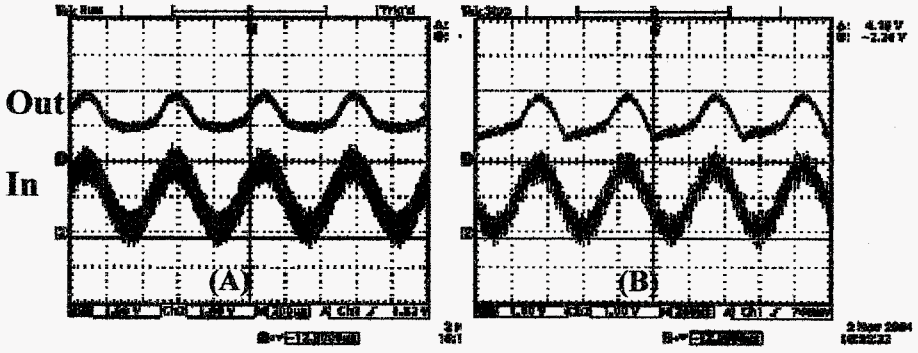


Figure 4: Half-wave rectifier evolved at -196C (A); solution is not robust and degrades when returned to room temperature (B). An environmental noise signal is also present at the circuit input.

NOR Gate

A NOR gate was evolved at -196.6°C using the same method described in section 3.2. Two FPTA cells were used and the experiment processed 100 individuals along 300 generations. Figure 5.a shows the oscilloscope picture of the evolved solution at -196.6°C. The same solution was tested at room temperature using another FPTA chip, producing an almost identical behavior (Figure 4.b) opposing to the rectifier case study.

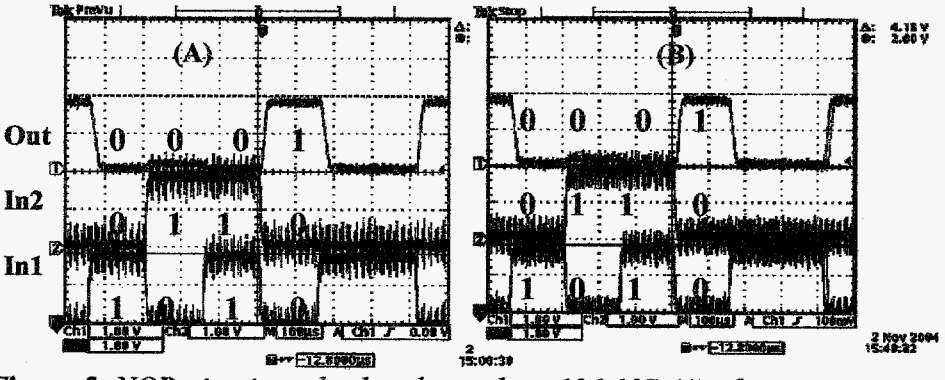


Figure 5. NOR circuit evolved and tested at -196.6℃ (A); the same circuit was tested successfully at roo temperature (B). An environmental noise signal is also present at the circuit input.

Recovery of Controllable Oscillator at Low Temperatures

Four cells of the FPTA were used to evolve a controllable oscillator. This circuit receives a digital input and it should oscillate when the input is at one digital level (either '0' and '1') and stay at ground for the other level. Initially, a controllable oscillator was evolved at room temperature, the circuit behavior being depicted in Figure 6.a. The circuits outputs a 70kHz sine wave (with a small degree of harmonic components) when the input is '0'. When the same circuit is tested at -196.6°C, it can be observed a distortion (increase in harmonics) at the output (Figure 6.b).

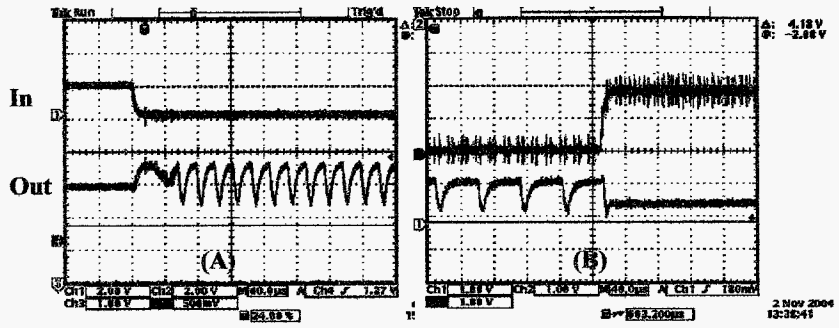


Figure 6: Evolved controllable oscillator at room temperature and deteriorated response at -196.6°C.

The controllable oscillator was evolved again at -196.6°C, the response being displayed in Figure 7. It can be observed that the output distortion largely removed. In addition, evolution found a circuit that oscillates for a high level input, opposing to the room temperature solution.

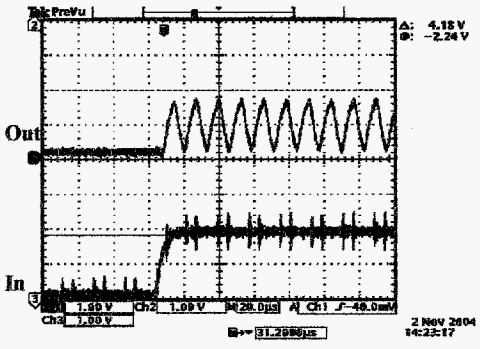


Figure 8. Evolved controllable oscillator at low temperature.

Testing of Virtex II Pro FPGA evaluation board under extreme environments:

The prototype Xilinx's commercial board (Virtex II Pro) was used to evaluate FPGA in our tests. The board was powered by 3 independent power supplies (3.3V, 2.5V and 1.5V DC). The 3.3V (Vcc-aux) powered the electronics in the board. The 2.5V (Vcco and MGT_VCC) provides power to I/O's, banks, and Rocket I/O transceivers. And the 1.5V (Vcore) supplies voltage to the FPGA Core.

The objective of this test was to learn survivability of the Virtex II Pro and its FPGA device (XC2VP20-FF1152BGB0325) under extreme temperatures. In our tests the board was taken from room temperature to +120°C and room temperature to -191°C with a ramp rate of 5°C/min. The chamber was set to various temperatures and stabilized at a set temperature and the board was tested during dwell time at the set temperature.

As discussed in the first test, a few modifications were made to the prototype board. One such change was to use a signal generator to replace the crystal oscillators (See Figure 7).The signal generator was adjusted at 100MHz with a D.C. offset of 500mV. This change was necessary to prevent any noise interference due to temperature fluctuations. Also Reset and Program Switch were brought out using push buttons (See Figure 7). The Reset switch allows the logic in the board to be reset after configuration. The Program Switch loads for the first time the program from the PROMS into the FPGA after configuration. In addition to the discussed changes, a new modification was added to the board for this test. The clocks were wired independently in the Prototyping Area of the board and their outputs were brought out to an Oscilloscope to see how much the signal was distorted. Test results are presented and discussed in the following pages.

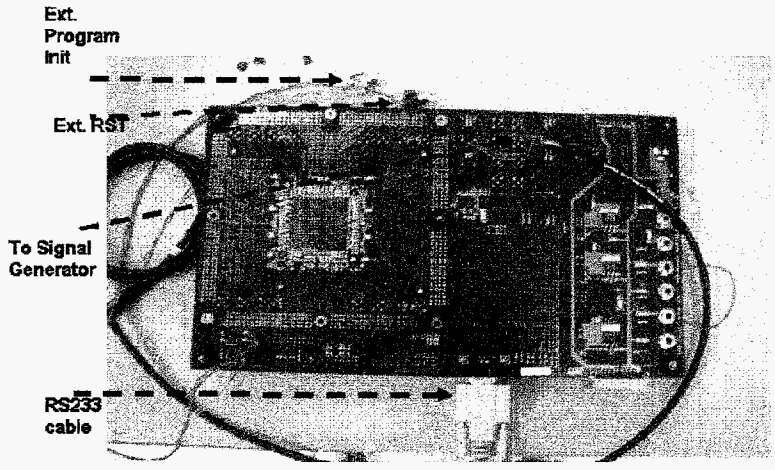


Figure 7: Optical photograph of Virtex II Pro evaluation board

Equipment: The equipment used to provide power and measurements for this test are Fluke 87 III DMM, HP 8110A 150MHz Pulse generator, one HP6641A D.C. Power supply, two Agilent E3633A D.C Power Supplies, one AM503B Current Probe Amplifier, 2 Oscilloscope Tektronix TDS3054B Scope 500Mhz (one to monitor the

clocks behavior, and the other one to read the in rush current of the FPGA core), and a Fluke 52II Thermometer with 2 "E" type thermocouples; these in addition to the thermocouple in the chamber (T0). To monitor the FPGA's temperature one of the thermocouples was taped to the heat sink case and this measurement is call "T2" and the second thermocouple was taped to the board T1. Also a small "Hello World" program was used to monitor the performance of the FPGA using Hyper-terminal to display it.

Low Temperature Test: The following values were measured before the test at room temperature and it was also tested in the chamber prior to closing. The values below were very constant in and out of the chamber (these are not power-on/transient values).

1. V = 3.3V at 110mA.
2. V = 2.5V between 35mA and 41mA.
3. V = 1.5V at 221mA.

The first test that was done by lowering the temperature of the FPGA evaluation board. See Figure 8 and 9 for chamber set up.

Figure 8: FPGA Evaluation board in the chamber; **Figure** 9: T0 thermocouple in the chamber.

The test was started and the chamber was closed with the board greeting the world and waiting for temperature to drop to its set temperature. The temperature began to drop from ambient (25°C) to 0°C. Once it reached the set target temperature it dwelled there for 5 minutes before descending to the next set target temperature. Measurement of the 3 thermocouples and voltages were recorded all through out the temperature changes and also the power cycling test was performed. The board was reset and it had worked. Then it was powered Off and On to make sure that it still worked. This test was performed all the way down to -120°C very successfully. Figure 10 shows the V_{core} In Rush current measured at room temperature.

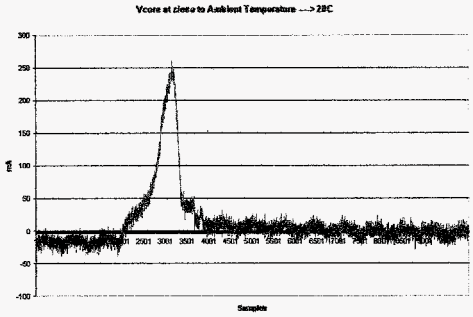


Figure 10: V_{core} In Rush current at ambient temperature

Temperatures T0 = 0.4°C T1 = 0.5°C and T2 = 0.8°C
V = 3.3V at 110mA. V = 2.5V at 41mA V = 1.5V at 210mA.

The next temperature in the target was -20°C. Recording for the Temperature and Voltages parameter were as follow:

Temperatures T0 = -19.8°C T1 = -19.6°C and T2 = -19.3°C
V = 3.3V at 110mA. V = 2.5V at 41mA V = 1.5V at 210mA.

Figure 11- 15 show a spreadsheet capture of the Vcore In rush current at "Power ON" at various temperatures.

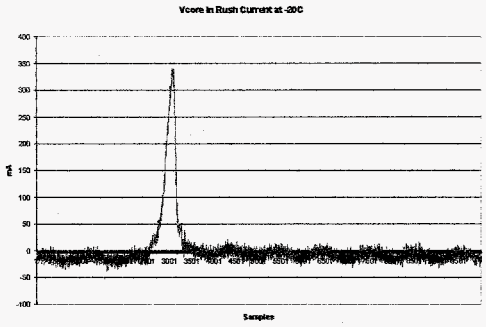


Figure 11: V_{core} In Rush Current at -20°C

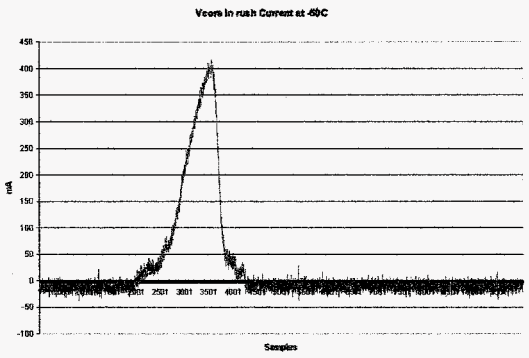


Figure 12: V_{core} In Rush Current at -60°C

Next temperature measured was -40°C.
Temperatures T0 = -40°C T1 = -40.3°C and T2 = -39.8°C
V = 3.3V at 110mA. V = 2.5V at 41mA V = 1.5V at 210mA.

Next temperature measured was -60°C.
Temperatures T0 = -60.1°C T1 = -60.3°C and T2 = -59.8°C
V = 3.3V at 110mA. V = 2.5V at 41mA V = 1.5V at 210mA.

Next temperature measured was -80°C.

Temperature T0 = -77.3°C T1 = -77.8°C and T2 = -77.8°C
V = 3.3V at 110mA. V = 2.5V at 41mA V = 1.5V at 210mA.

Next temperature measured was -100°C.
Temperature T0 = -100.8°C T1 = -100.9°C and T2 = -96.5°C
V = 3.3V at 110mA. V = 2.5V at 39mA V = 1.5V at 210mA.

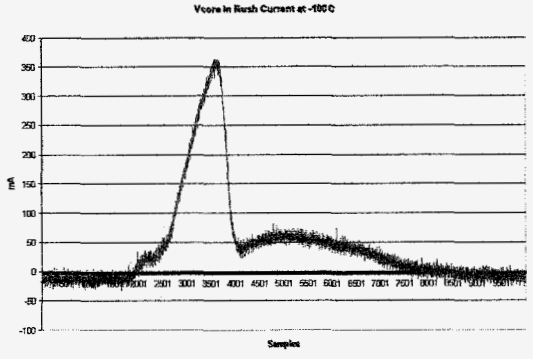


Figure 13: V_{core} In Rush Current at -120°C

Next temperature measured was -120°C.
Temperature T0 = -121.7°C T1 = -122.2°C and T2 = -120.1°C
V = 3.3V at 110mA. V = 2.5V at 39mA V = 1.5V at 210mA.

Next temperature measured was -140°C.
Temperature T0 = -143.5°C T1 = -144.4°C and T2 = -140.9°C
V = 3.3V at 110mA. V = 2.5V at 38mA V = 1.5V at 211mA.

Since it was not known whether the board would successfully reset and pass the Power OFF/ON test, it was decided to reset first and then cycle the power to verify validity of this test. At this particular temperature both worked.

Next temperature measured was -160°C.
Temperature T0 = -161°C T1 = Over Loaded T2 = Over Loaded
V = 3.3V at 110mA. V = 2.5V at 38mA V = 1.5V at 210mA.

At this temperature the Thermometer was overloaded and couldn't read the temperatures due to the thermocouples qualification (-150 °C to 1000 °C). Another observation was that the clocks were clear and they had no noise interference.

Next temperature measured at -180°C.
Temperature T0 = -121.7°C T1 = -122.2°C T2 = -120.1°C
V = 3.3V at 110mA. V = 2.5V at 38mA V = 1.5V at 210mA.

Those were the readings until the board was powered down and failed to come back with its "Hello World" program. Nothing worked from Reset to Program Initialization (re-loading the PROMS). After many attempts to bring it back with out any success, it was decided to warm up the chamber's temperature at 1°C/min. At about -146°C the power cycling worked and the board came back alive with its message (Hello World). At this point it was decided to let the board run without any further power cycling test. The clocks worked and the following is a measurement of the Vcore Transient Current.

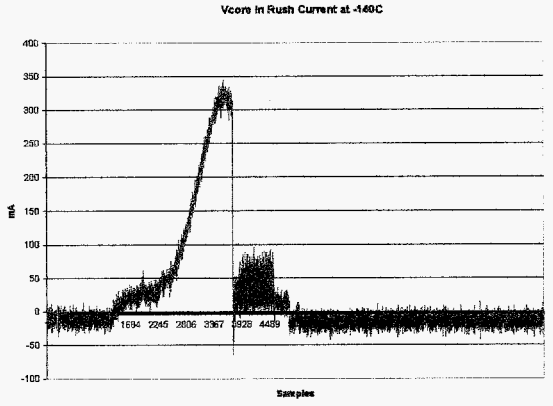


Figure 14: V_{core} In Rush Current at -140°C

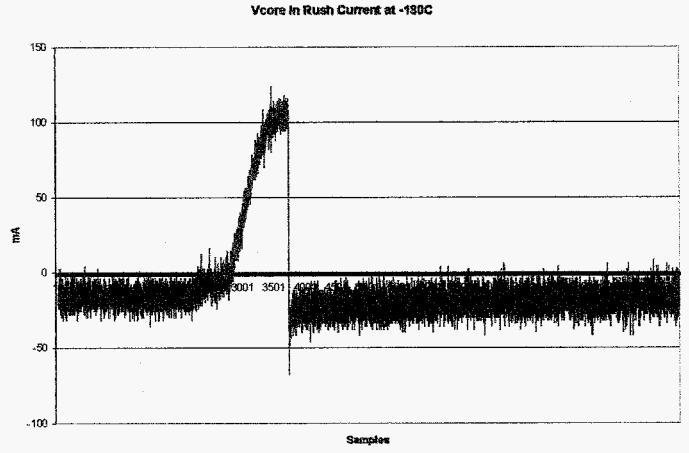


Figure 15: V_{core} In Rush Current at -180°C

As it can be observed that the Transient Current diminished until it no longer can supply to the board what it needs due to the low temperature.

Next temperature measured at -190°C.

Temperature T0 = -191.9°C T1 = Over Loaded T2 = Over Loaded
V = 3.3V at 110mA. V = 2.5V at 38mA V = 1.5V at 215mA.

The temperature was brought up to ambient and at that point, the low temperature test concluded. It was noticed at the end of this test that the Transient Current was pretty much the same up to -160°C and it lasted between 25msec-30msec at the most. It is still a bit obscure which component in the board failed, whether it was the PROMS or the FPGA. Further study and test needs to be done to determine this, such as having only the FPGA inside the Chamber and everything else outside at room temperature to conclude with certainty that it is the FPGA the one failing at this temperature.

High Temperature Test: The chamber where the Virtex Pro II was kept closed, and everything was set up during the "Low Temperature Test". Figure 16- 17 show a spreadsheet capture of the Vcore In rush current at "Power ON" at various temperatures.

Initial Temperature inside the chamber was + 45.7°C.
Temperature T0 = +45.7°C T1 = 45.8°C T2 = 46°C
V = 3.3V at 110mA. V = 2.5V at 60mA V = 1.5V at 215mA.

Next temperature measured at +60°C.
Temperature T0 = + 60.8°C T1 = + 59.6°C T2 = + 56.3°C
V = 3.3V at 110mA. V = 2.5V at 60mA V = 1.5V at 230mA.

Next temperature measured at +80°C.
Temperature T0 = + 80.4°C T1 = + 80°C T2 = + 75.7°C
V = 3.3V at 108mA. V = 2.5V at 60mA V = 1.5V at 238mA.

The clocks are working as expected. Reset and Program Initialization as well as the Power cycling worked.

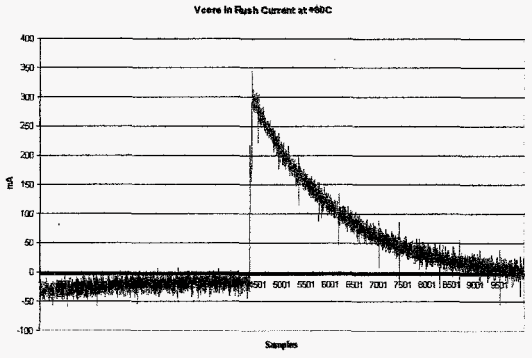


Figure 16: V_{core} In Rush Current at 80°C

Next temperature measured at +100°C.
Temperature T0 = + 101.4°C T1 = + 99.4°C T2 = + 93.5°C
V = 3.3V at 110mA. V = 2.5V at 60mA V = 1.5V at 348mA.

Clocks worked without any problems. Reset, Program Initialization, and Power cycling came back alright.

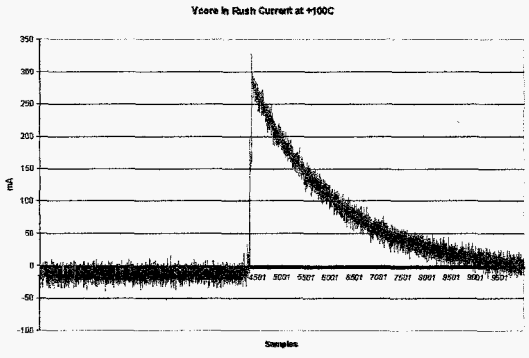


Figure 17: V_{core} In Rush Current at 100°C

Next temperature measured at +120°C.
Temperature T0 = + 120.3°C T1 = + 119.3°C T2 = + 115.3°C
V = 3.3V at 111mA. V = 2.5V at 60mA V = 1.5V at 348mA.

Clocks worked without any problems. Reset, Program Initialization, and Power cycling came back alright. At this point the board reached its target temperature and now it is necessary to bring the temperature down to ambient and verify that the board is still working. Pretty much from this temperature on until it reaches +40°C, all of this test worked without any problem.

Next temperature measured at +100°C.
Temperature T0 = + 100.3°C T1 = + 101.9°C T2 = + 103.4°C
V = 3.3V at 110mA. V = 2.5V at 58mA V = 1.5V at 348mA.

Next temperature measured at +80°C.
Temperature T0 = + 77.7 °C T1 = + 77.3°C T2 = + 85.4°C
V = 3.3V at 108mA. V = 2.5V at 58mA V = 1.5V at 313mA.

Next temperature measured at + 60°C.
Temperature T0 = + 53.5°C T1 = + 52.6°C T2 = + 64.2°C
V = 3.3V at 110mA. V = 2.5V at 58mA V = 1.5V at 310mA.

Next temperature measured at +40°C.
Temperature T0 = + 39.5°C T1 = + 35.8°C T2 = + 47.2°C
V = 3.3V at 108mA. V = 2.5V at 38mA V = 1.5V at 298mA.

At this temperature the Board stopped working. The Chamber was open and it was found that the BNC connector that was solder to the board came undone (the clock connector). It is believed that the solder didn't hold well due to temperature stress/thermal stress. To

prepare for the second attempt and to avoid the same problem as before, it was decided to use the 100MHz oscillator chip and repeated the tests at high temperature.

All Temperatures, Voltages and Current registered normal as well as Power cycling, reset and program initialization. There was a little difference between the two tests at high temperature in the Vcore. The Vcore for example in test 2 at + 120°C was 348mA for the day one and 327mA for the second day. Over all the High Temperature Transient have sharper current, take less effort to come back and last less than the Cold Temperature which is expected. Transient for Vcore was approximately most of the time at around 180mA for about 15-20msec.

Reconfigurable Analog Array Component Testing in Extreme Environments: We have tested the behavior of Gm-C filter building blocks at extreme temperatures (from -180°C to 120°C). We have also performed preliminary tests on the functionality recovery through changes in the voltage bias; Components tested (Designed by SPAWAR using TSMC 0.35µm technology): Operational transconductance amplifier (OTA); wide range OTA (WRTA), single-ended first order Gm-C filter.

OTA characteristics: Current lower and upper limits reduce as the temperature reduces as observed in Figure 18. Device function can be recovered by increasing Vb from 0.8V to 0.85V as observed experimentally and shown in the Figure 19. Negative and positive saturation voltages increase as the temperature gets higher as shown in Figure 20. Device function can be recovered by decreasing Vb from 0.8V to around 0.75V as shown in Figure 21.

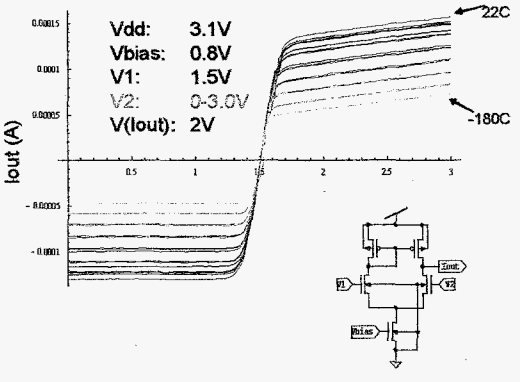


Figure 18: OTA Sweep Down (23°C to -180°C)

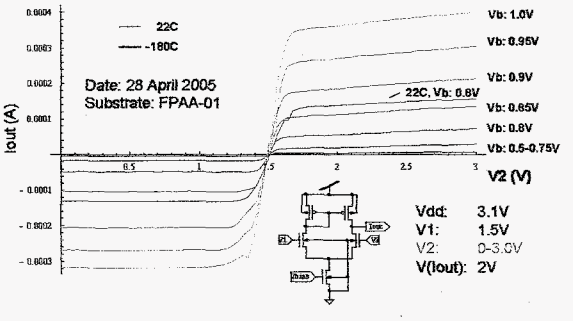


Figure 19: OTA Bias Sweep at -180°C

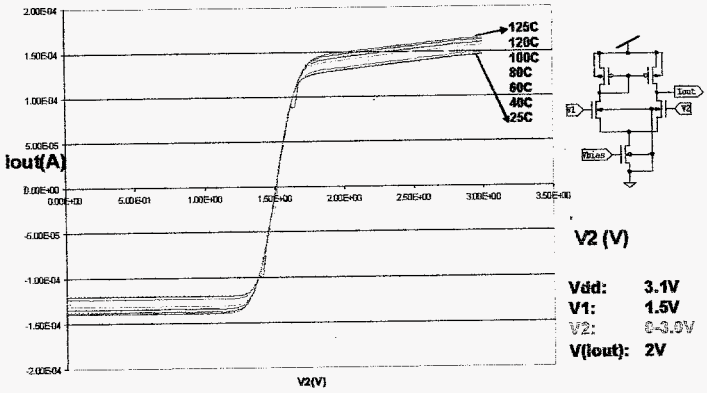


Figure 20: OTA Sweep Up (25°C to 125°C)

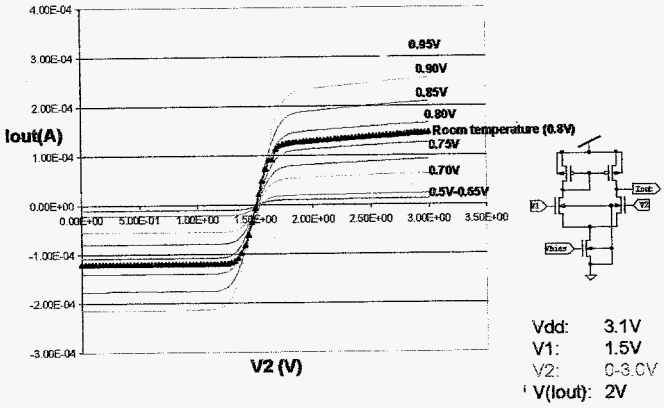
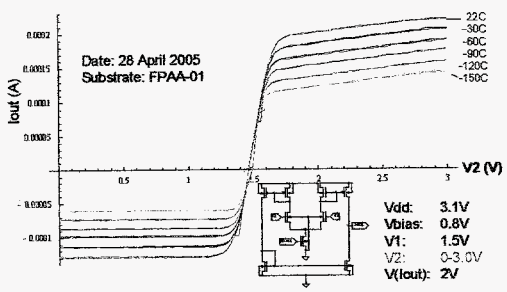


Figure21: OTA Bias Sweep at 120°C

WRTA Characteristics: Current lower and upper limits reduce as the temperature reduces as observed in the Figure 22. Device function can be recovered by increasing Vb from 0.8V to 0.85V as observed the experimental shown in the Figure 23



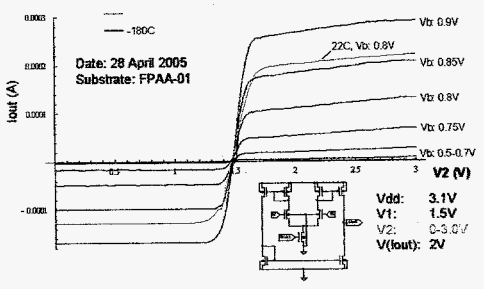


Figure 22: WRTA Sweep Up (-180°C to 22°C) **Figure 23**:WRTA Bias Sweep @ -180°C

First Order GmC Low Pass Filter: Test the recovery through Vbias in a filter circuit (Figure 24); built at the board level using two chips (two OTAs); Characterize filter behavior at extreme temperatures and test recovery through adjustment of bias voltage;

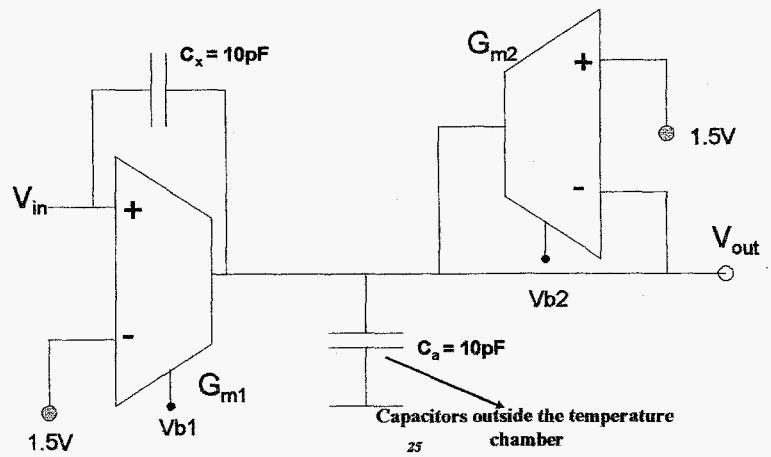


Figure 24: First Order GmC Low Pass Filter

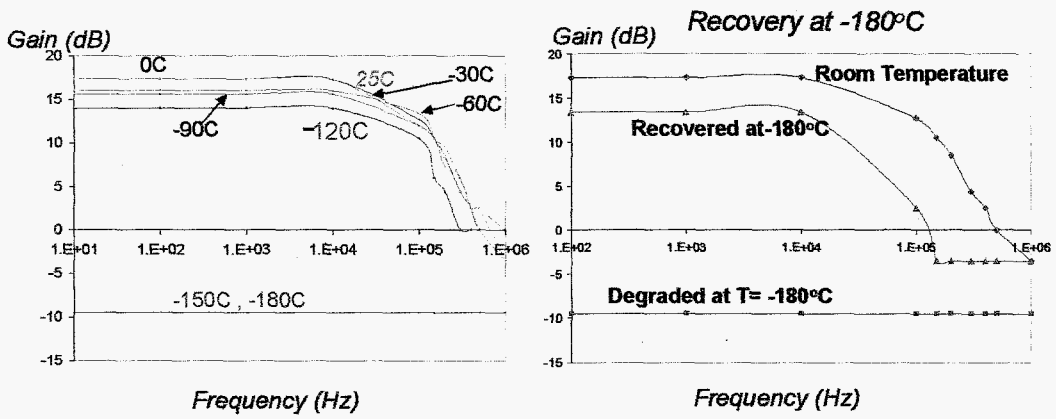


Figure 25: Filter Recovery at -180°C

It can be observed from Figure 25 that the filter behavior completely degrades to a flat response when the temperature reduces below -120°C (left graph). A partial recovery of

the filter response was performed at -180°C through a manual local search over the values of Vb1 and Vb2 (right graph). The partial recovery resulted from changing Vb1/Vb2 from 0.9V/0.7V to 0.8V/0.7V. A complete recovery of the filter response could be obtained by sweeping Vb1 and Vb2 using finer steps and/or implementing a non-local search algorithm.

Conclusions and Future Work

The results summarized above prove the concept, yet have the following limitations: 1) the tests were of short duration, 2) did not implement temperature cycling, 3) did not use the combined EHW system (DSP and FPTA) at low temperature simultaneously, 4) were not demonstrated on complex analog or digital circuits performing in an application. Particularly, the DSP Board worked down to -110°C, but failed for further lower temperatures.

Results indicate that bias voltage control adjustment is an efficient mechanism for circuit recovery at extreme temperatures. Small changes in the bias voltage are sufficient to promote functionality recovery of the OTA and WRTA devices tested at low and high temperatures; Low Pass filter recovery was also possible through changes in the bias voltages → more systematic search methods and/or algorithms needed to further improve recovered function.

Longer term goals planned for this effort are: demonstrate the integrated reconfigurable array-reconfiguration logic in the same chip under temperatures cycles accurately replicating those in Moon and Mars and for longer duration and in combined radiation/temperature tests, performing a sensor processing function. More specifically, the overall objective of the new effort is to develop/demonstrate reconfigurable analog electronics performing characteristic analog functions (filtering, amplification, etc) for extended operations in extreme environment with temperatures cycling in the range of –180°C and 120°C and cumulative radiation of at least 300kRad total ionizing dose (TID). The objective is to develop and validate Self Reconfigurable Electronics for Extreme Environments (SRE-EE) technology by demonstrating a Self-Reconfigurable Analog Array (SRAA) IC in sustained (over 200 hours) operation at temperatures between -180°C and 120°C, and irradiated to 300KRad total ionizing dose (TID). The temperature range of -180°C and 120°C covers the temperature range for both Moon and Mars environments and 300KRad TID reflects accumulative dose during very long Mars missions (100KRad for near-term missions), or missions beyond the Moon and Mars, such as to Jupiter's Moons. This would validate the technology for Moon and Mars temperature and radiation environments and the even harsher radiation environments for missions beyond

Acknowledgement

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